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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NGUYEN, KHIEM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/945,084

Applicant(s)

FOGAL ET AL.

Examiner

Khiem D Nguyen

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-- **Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 and 24-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 and 24-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-19 in Paper No. 6 is acknowledged.

Claims 19-23 have been canceled as being non-elected and claims 24-27 have been added. Claims 1-19 and 24-27 remain pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2, 8, 11, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (U.S. Pub. 2002/0020058).

In re claims 1, 8, 11, 15, and 17, Saito discloses a method used to form a semiconductor device comprising: providing a semiconductor wafer section comprising a bond pad having first and second portions which are electrically separated; providing a first circuit portion (FIG. 6, 4) electrically coupled with the first bond pad portion (FIG. 6, 5); providing a second circuit portion (FIG. 6, 7) electrically coupled with the second bond pad (FIG. 6, 1, 3) and electrically isolated from the first circuit portion; and electrically connecting the first and second pad portions to electrically connect the first and second circuit portions.

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In re claim 2, Saito discloses attaching a ball bond (FIG. 6, 6) to the first (FIG. 6, 5) and second bond pad (FIG. 6, 1, 13) during electrically connecting of the first and second pad portions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-7, 9-10, 12-14, 16, 18-19, and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pub. 2002/0020058) as applied to claims 1-2, 8, 11, 15 and 17 above, and further in view of Johnston (U.S. Patent 5,898,217) and the applicant's admitted prior art (AAPA) of this application.

In re claims 3-4 and 14, Johnston discloses attaching a wire bond (FIG. 2, 128a) to the first (FIG. 2, 121) and second (FIG. 2, 132) bond pad portions during electrically connecting of the first and second pad portions and screen printing a conductive epoxy (FIG. 2, 113) to the first and second bond pad portions during electrically connecting of the first and second pad portions (col. 2, line 53 to col. 3, line 19). It would have been obvious to one of ordinary skill in the art to combine the teaching of Saito and Johnston to enable the process of attaching a wire bond and screen printing a conductive epoxy to the first and second bond pad portions of Saito to be performed.

In re claims 5, 13 and 24-27, Saito teaches providing a third bond pad and a third circuit portions, wherein the third pad portion is electrically coupled with the third circuit

portion and is electrically isolated from the first and second circuit portions and during electrically connecting the first and second pad portions, electrically connecting the first, second, and third pad portions to electrically connect first, second, and third circuit portions. Saito teaches providing a third bond pad and a third circuit portions. In figure 9, the bridge 12 display a ball joint between two pads, but this is heuristic. Saito in page 4, paragraphs [0065]-[0066], notice that the bridges could include the bonding between other pads in the third dimension or between multiple pads.

In re claim 6, AAPA disclose providing a transistor during providing the first circuit portion and providing one of a fuse and antifuse array during providing of the second circuit portion and electrically couple one of the fuse and antifuse array to the transistor during electrical connection of the first and second bond pad portions (Background of the Invention on pages 2-3, paragraph [0005] and FIG. 1 of this application). It would have been obvious to one of ordinary skill in the art to combine the teaching of Saito and AAPA to electrically couple the fuse and antifuse array to the transistor during electrical connection of the first and second bond pad portions.

In re claims 7 and 12, AAPA discloses providing a lead frame and subsequent to electrically connecting the first and second pad portions, attaching the wafer section to the lead frame (page 4, paragraph [0010]).

In re claims 9 and 10, AAPA discloses electrically coupling the second pad portion to the voltage source through a probe tip during the electrical coupling of the second pad portion with the voltage source; providing a CGND node during providing of second pad portion; electrically coupling the CGND node to the transistor during

electrical coupling of the first pad portion with the second pad portion; and tying the CGND node to ground through the transistor during an operational mode of the semiconductor device subsequent to programming the array (pages 2-3, paragraph [0005] and FIG. 1).

In re claims 16, 18 and 19, AAPA discloses encapsulating the semiconductor wafer substrate assembly subsequent to selection of operational mode; forming a V_{SS} power buss and a V_{SSQ} power buss during formation of the first and second internal power buses; and electrically connecting the first conductive pad with the second conductive pad to electrically connect the V_{SS} power bus with the V_{SSQ} power bus (pages 2-4, paragraphs [0004]-[0010]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.

July 15, 2003



Chik Chao
Supervisory Patent Examiner
Technology Center 2800